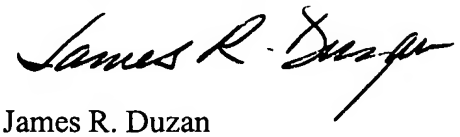
REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth hereto prior to examination of the application on the merits.

Respectfully submitted,



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JRD/tlb

VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

[0001] This application is a continuation of application Serial No. 09/211,089, filed December 14, 1998, [pending]now U.S. Patent No. 6,342,789 B1, issued 1/29/2002, which is a divisional of application Serial No. 08/643,518, filed May 6, 1996, now U.S. Patent 5,905,382, issued May 18, 1999, which is a continuation of application Serial No. 07/981,956, filed November 24, 1992, now U.S. Patent 5,539,324, which is a continuation-in-part of application Serial No. 07/575,470, filed August 29, 1990, abandoned, and shares common subject matter with copending applications 07/709,858 and 07/788,065.

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) [An]A testing apparatus for a wafer of semiconductor dice comprising:

a first rigid support member for receiving a plurality of semiconductor dice in wafer form having a predetermined orientation, the first rigid support member having a plurality of contact members thereon and having a plurality of electrical connectors connected to the contact members for establishing communication with test circuitry;

a second rigid support member for selectively engaging the first rigid support member to retain the plurality of semiconductor dice in wafer form therebetween, one of the first rigid support member and the second rigid support member including a single cavity for retaining [said]the semiconductor dice in wafer form therein during testing; and

a single biasing assembly including a single floating platform of a preselected area substantially sized for [said]the single cavity, the single biasing assembly mounted to one of the first rigid support member and second rigid support member, the single biasing assembly sized for uniformly biasing [said]the plurality of semiconductor dice in wafer form against the contact members.

6. (Amended) A wafer testing apparatus comprising:

a first rigid support member and a second rigid support member for receiving a wafer therebetween, one of the first rigid support member and second rigid support member including a single cavity for retaining the wafer therein during testing;

a plurality of contact members formed on the first rigid support member for communicating with electrical connectors for connecting to external test circuitry;

a single biasing assembly including a single floating platform having a preselected area substantially sized to correspond with [said]the single cavity and an elastomeric member disposed on the second rigid support member, the single biasing assembly sized for uniformly biasing the wafer towards the contact members, the single floating platform

directly supporting the wafer [having]with the elastomeric member sandwiched between the single floating platform and the second rigid support member.

8. (Amended) The apparatus as claimed in claim 6, further comprising an alignment device including a dowel on one of the first rigid support member and second rigid support member and a corresponding opening on the other of the first rigid support member and the second rigid support member.